Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
		"22" and (memory RAM ROM SRAM SROM DRAM DROM CAM Flash EPROM EEPROM cache)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/04 14:32
		"22" and (memory RAM ROM SRAM SROM DRAM DROM CAM Flash EPROM EEPROM cache	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/04 14:32
		(test synchron$4 logic) near (controller)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2003/03/04 13:36
S1	8	"deskew controller"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2003/03/04 13:23
S2	15502	(test synchron$4 logic) near (controller)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/05 11:54
S3	2	"5253255".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/04 13:41
S4	12973	(test logic) near (controller)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/04 14:13
S5	371	((test synchron$4 logic) near (controller)) and (test adj (bus port "access port" access))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/04 14:34
S6	99	(((test synchron$4 logic) near (controller)) and (test adj bus)) and ((transmission data information instruction) near (bits))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/04 15:01

S7	371	((test synchron$4 logic) near (controller)) and (test adj (bus port "access port" access))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/04 14:35
S8	1	((((test synchron$4 logic) near (controller)) and (test adj (bus port "access port" access))) and ((transmission data information instruction) near (bits))) and (deskew de-skew)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/04 15:11
S9	198	(((test synchron$4 logic) near (controller)) and (test adj (bus port "access port" access))) and ((transmission data information instruction) near (bits))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/05 09:10
S10	0	"n = a + log.sub.2 i"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/04 15:26
S11	735	710/305.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2003/03/05 12:15
S12	68	710/305.ccls. and (((instruction command rule control) near (bit bits data signal signals)) and ((information data) near (bit bits data signal signals)) and (bit near (lines line row rows columns column)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/05 11:54
S13	779	((test synchron$4 logic) near (controller)) and ("log")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/05 12:16
S14	46	710/305.ccls. and ("log")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/05 12:08
S15	46	"IEEE 1149.1" and "log"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/05 12:15

S16	0	710/305.ccls. and ("log" near ("2" "two"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/05 12:16
S17	24	((test synchron$4 logic) near (controller)) and ("log" near ("2" "two"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/05 12:17
S18	1	"IEEE 1149.1" and ("log" near ("2" "two"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/05 12:17
S19	14	("5132685" "5173906" "5553082" "5568437" "5617531" "5764878" "5812562").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/03 12:59
S20	7	("5132685" "5173906" "5553082" "5568437" "5617531" "5764878" "5812562").pn.	USPAT	OR	ON	2004/11/03 13:02
S21	5	("5132685" "5173906" "5553082" "5568437" "5617531" "5764878" "5812562").pn. and ((manufacturing board system) near (test$3))	USPAT	OR	ON	2004/11/03 13:03
S22	0	("5132685" "5173906" "5553082" "5568437" "5617531" "5764878" "5812562").pn. and ((manufacturing board system) near (test$3) near level)	USPAT	OR	ON	2004/11/03 13:03
S23	275	((manufacturing board system) near (test$3) near level)	USPAT	OR	ON	2004/11/03 13:03
S24	57	((manufacturing board system) near (test$3) near level) and ("built-in self-test" "self-test" BIST)	USPAT	OR	ON	2004/11/03 13:04
S25	1	((manufacturing and board and system) near (test$3) near level) and ("built-in self-test" "self-test" BIST)	USPAT	OR	ON	2004/11/03 13:04
S26	99	(((test synchron$4 logic) near (controller)) and (test adj bus)) and ((transmission data information instruction) near (bits))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/04 14:28

S27	91	((((test synchron$4 logic) near (controller)) and (test adj bus)) and ((transmission data information instruction) near (bits))) and (memory RAM ROM SRAM SROM DRAM DROM CAM Flash EPROM EEPROM cache)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/04 14:32
S28	158	((test synchron$4 logic) near (controller)) and (test adj bus)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2003/03/04 14:24